CLAIMS:

What we claim is:

1. A multiply-accumulate module comprising:

a multiply-accumulate core, wherein said multiply-accumulate core comprises:

a plurality of Booth encoder cells;

a plurality of Booth decoder cells connected to at least one of said Booth encoder cells; and

a plurality of Wallace tree cells connected to at least one of said Booth decoder cells, wherein at least one first Wallace tree cell or at least one first Booth decoder cell comprises a first plurality of transistors, and at least one second Wallace tree cell or at least one second Booth decoder cell comprises a second plurality of transistors, wherein at least one critical path of said multiply-accumulate module comprises said at least one first cell and a width of at least one of said first plurality of transistors is greater than a width of at least one of said second plurality of transistors.

2. The multiply-accumulate module of claim 1, wherein none of said critical paths of said multiply-accumulate module comprises said at least one second cell.

3. The multiply-accumulate module of claim 1, wherein said multiply-accumulate core further comprises:

an adder connected to at least one of said Wallace tree cells;

a saturation detector connected to said adder, wherein said multiply-accumulate module further comprises:

at least one input register connected to at least one of said Booth encoding cells; and

at least one result register connected to said saturation detector, wherein said critical path is an electrical path for which an amount of time that it takes for an electrical signal to travel from said at least one input register to said at least one result register is greater than or equal to a predetermined amount of time, wherein said predetermined amount of time is less than a longest amount of time that it takes any other electrical signal to travel from said at least one input register to said at least one result register.

4. The multiply-accumulate module of claim 1, wherein said at least one first cell comprises said first Wallace tree cell, said at least one second cell comprises said second Wallace tree cell,

said at least one first cell is connected to and powered by a first power supply, and said at least one second cell is connected to and powered by said first power supply.

5. The multiply-accumulate module of claim 1, wherein said at least one first cell comprises said first Booth decoder cell, said at least one second cell comprises said second Booth decoder cell, said at least one first cell is connected to and powered by a first power supply, and said at least one second cell is connected to and powered by said first power supply.

6. The multiply-accumulate module of claim 1, wherein said at least one first Wallace tree cell and said at least one first Booth decoder cell comprise said first plurality of transistors, and said at least one second Wallace tree cell and said at least one second Booth decoder cell comprise said second plurality of transistors.

7. The multiply-accumulate module of claim 1, wherein said width of each of said first plurality of transistors is greater than said width of each of said second plurality of transistors.

8. The multiply-accumulate module of claim 4, wherein said amount of time that it takes for said electrical signal to travel from said at least one input register to said at least one result register through said critical path comprising said at least one first cell is a first amount of time, and an amount of time that it takes for said electrical signal to travel from said at least one input register to said at least one result register through a non-critical path comprising said at least one second cell is a second amount of time, wherein said width of said at least one of said first plurality of transistors is selected such that said first amount of time is greater than or equal to said second amount of time.

9. The multiply-accumulate module of claim 1, wherein said at least one second cell is a most significant bit or a least significant bit and said at least one first cell is not a most significant bit or a least significant bit.

10. A parallel multiplier comprising:

a parallel multiplier core, wherein said parallel multiplier core comprises:

a plurality of Booth encoder cells;

a plurality of Booth decoder cells connected to at least one of said Booth encoder cells; and

a plurality of Wallace tree cells connected to at least one of said Booth decoder cells, wherein at least one first Wallace tree cell or at least one first Booth decoder cell comprises a first plurality of transistors, and at least one second Wallace tree cell or at least one second

Booth decoder cell comprises a second plurality of transistors, wherein at least one critical path of said parallel multiplier comprises said at least one first cell and a width of at least one of said first plurality of transistors is greater than a width of at least one of said second plurality of transistors.

11. The parallel multiplier of claim 10, wherein none of said critical paths of said parallel multiplier comprises said at least one second cell.

12. The parallel multiplier of claim 10, wherein said parallel multiplier core further comprises:

an adder connected to at least one of said Wallace tree cells;

a saturation detector connected to said adder, wherein said parallel multiplier further comprises:

at least one input register connected to at least one of said Booth encoding cells; and

at least one result register connected to said saturation detector and at least one of said Wallace tree cells, wherein said critical path is an electrical path for which an amount of time that it takes for an electrical signal to travel from said at least one input register to said at least one result register is greater than or equal to a predetermined amount of time, wherein said predetermined amount of time is less than a longest amount of time that it takes any other electrical signal to travel from said at least one input register to said at least one result register.

13. The parallel multiplier of claim 10, wherein said at least one first cell comprises said first Wallace tree cell, said at least one second cell comprises said second Wallace tree cell, said at least one first cell is connected to and powered by a first power supply, and said at least one second cell is connected to and powered by said first power supply.

14. The parallel multiplier of claim 10, wherein said at least one first cell comprises said first Booth decoder cell, said at least one second cell comprises said second Booth decoder cell, said at least one first cell is connected to and powered by a first power supply, and said at least one second cell is connected to and powered by said first power supply.

15. The parallel multiplier of claim 10, wherein said at least one first Wallace tree cell and said at least one first Booth decoder cell comprise said first plurality of transistors, and said at least one second Wallace tree cell and said at least one second Booth decoder cell comprise said second plurality of transistors.

16. The parallel multiplier of claim 10, wherein said width of each of said first plurality of transistors is greater than said width of each of said second plurality of transistors.

17. The parallel multiplier of claim 12, wherein said amount of time that it takes for said electrical signal to travel from said at least one input register to said at least one result register through said critical path comprising at least one first cell is a first amount of time, and an amount of time that it takes for said electrical signal to travel from said at least one input register to said at least one result register through a non-critical path comprising at least one second cell is a second amount of time, wherein said width of said at least one of said first plurality of transistors is selected such that said first amount of time is greater than or equal to said second amount of time.

18. The multiply-accumulate module of claim 10, wherein at least one second cell is a most significant bit or a least significant bit and at least one first cell is not a most significant bit or a least significant bit.

19. A method of designing a multiply-accumulate module comprising the steps of:

providing a multiply-accumulate core, wherein the step of providing a multiply-accumulate core comprises the steps of:

providing a plurality of Booth encoder cells;

connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;

connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells, wherein at least one first Wallace tree cell or at least one first Booth decoder cell comprises a first plurality of transistors, and at least one second Wallace tree cell or at least one second Booth decoder cell comprises a second plurality of transistors, wherein at least one critical path of said multiply-accumulate module comprises at least one first cell;

selecting a first width for at least one of said first plurality of transistors; and

selecting a second width for at least one of said second plurality of transistors which is less than said first width.

20. A method of designing a parallel multiplier comprising the steps of:

providing a parallel multiplier core, wherein the step of providing a parallel multiplier core comprises the steps of:

providing a plurality of Booth encoder cells;

connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;

connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells, wherein at least one first Wallace tree cell or at least one first Booth decoder cell comprises a first plurality of transistors, and at least one second Wallace tree cell or at least one second Booth decoder cell comprises a second plurality of transistors, wherein at least one critical path of said multiply-accumulate module comprises at least one first cell;

selecting a first width for at least one of said first plurality of transistors; and

selecting a second width for at least one of said second plurality of transistors which is less than said first width.